What is claimed is:

1) A method of operating a digital tuner, comprising:

digitizing a first number of input signals to create respective streams of digitized input data;

providing a second number of per-channel front-ends for performing baseband translation and filtering in the digital domain and providing outputs suitable for subsequent demodulation;

providing each per-channel front-end with an input selector coupled to each of the streams of digitized input data; and

configuring each of the per-channel front-ends to process a selected one of the first number of streams of digitized input data.

2. A method of operating a digital tuner, comprising:

providing a first number of A/D converters for digitizing a first number of input signals to create respective streams of digitized input data;

providing each A/D converter with a preceding variable-gain amplifier;

setting the amplifier gain as a function of the entire carrier multiplex present on the input signals;

providing a second number of per-channel front-ends for performing baseband translation and filtering in the digital domain and providing outputs suitable for subsequent demodulation;

providing each per-channel front-end with a respective digital signal scaler coupled to a selected one of the streams of digitized input data;

providing the output of the scaler to the subsequent stages of its respective per-channel front-end; and

for each per-channel front-end, dynamically scaling the selected incoming stream of digitized input data as a function of the signal power of the desired carrier to minimize variations in the peak magnitude of the signals processed.

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3. A method of operating a digital tuner, comprising:

providing a first plurality of input signals having a second plurality of symbol rates;

providing a first sampling clock that is a common integer multiple of the second plurality of symbol rates;

digitizing the first plurality of input signals using the first sampling clock to create respective streams of digitized input data;

providing a third plurality of per-channel front-ends, each front-end having a baseband converter, a first decimator, and a matched filter;

operating the baseband converter and the first decimator of each per-channel front-end at the first sampling clock; and

for each per-channel front end, providing a selectively decimated number of samples to each matched filter and operating each matched filter at a selected compatible sampling clock, such that a constant number of symbol samples is output from each matched filter.

4. A digital tuner, comprising:

a first plurality of digitizers operating at a common first sampling rate and providing a first plurality of digitized data streams corresponding to a first plurality of analog inputs;

a second plurality of digital front-ends, each front-end including

selector circuitry for selectable coupling of one of the first plurality of digitized data streams to post-selector processing circuitry of the associated front-end, each selector operating independently of the other selectors,

digital frequency conversion circuitry having a selectable conversion frequency from a predetermined set of conversion frequencies, and

post-conversion circuitry having a selectable decimation factor from a predetermined set of decimation factors, the post-conversion circuitry providing an output suitable for subsequent processing by a digital demodulator; and

wherein configuration of the tuner may select any arbitrary combination of one of the first plurality of analog inputs, one of the set of conversion frequencies, and one of the set of decimation factors.

5. The digital tuner of claim 4, wherein the configuration of the tuner is accomplished programmatically.

6. The digital tuner of claim 4, wherein the configuration of the tuner is accomplished remotely.

7. The digital tuner of claim 4, wherein the configuration of the tuner is accomplished automatically.

8. The digital tuner of claim 4, wherein the configuration of the tuner is accomplished dynamically.

9. The digital tuner of claim 4, wherein the configuration of the tuner is accomplished without involving a human operator.

10. The digital tuner of claim 4, wherein the common first sampling rate is an integer multiple of each decimation factor of the predetermined set of decimation factors.

11. The digital tuner of claim 4, wherein each decimation factor of the predetermined set of decimation factors is an integer sub-multiple of the common first sampling rate.

12. The digital tuner of claim 4, wherein the post-conversion circuitry is implemented as a single stage having a configurable decimation factor selected from a predetermined set.

13. The digital tuner of claim 12, wherein the predetermined set includes decimation factors of 10, 20, 40, 80, and 160.

14. The digital tuner of claim 4, wherein the post-conversion circuitry is implemented as multiple stages of which some have a fixed decimation factor and others have a configurable decimation factor.

15. The digital tuner of claim 14, wherein the post-conversion circuitry is implemented using a first stage having a fixed decimation factor and a second stage having a configurable decimation factor selected from a predetermined set.

16. The digital tuner of claim 15, wherein the fixed decimation factor is 10.

17. The digital tuner of claim 15, wherein the predetermined set includes decimation factors of 1, 2, 4, 8, and 16.

18. The digital tuner of claim 15, wherein the fixed decimation factor is 10 and the predetermined set includes decimation factors of 1, 2, 4, 8, and 16.

19. The digital tuner of claim 4, wherein the post-conversion circuitry is implemented as multiple stages of which each has a configurable decimation factor.

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